AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A method for a ~~display controller~~ graphics chip to access data stored in a memory device of a computer device comprising:

setting a block capacity value;

dividing a plurality of read requests corresponding to a predetermined request sequence and said block capacity value into a plurality of request, wherein a total amount of data required by read requests grouped in each request group is less than the block capacity value; and

reordering the read requests in each of said request groups corresponding to data on the page of said memory device into a second request sequence for each of said request groups;

executing the read requests in each of request group according to said second request sequence of each of said request groups.

2. (Original) The method of claim 1 further comprising: when the pages accessed by the read requests in the next request group is as same as the page accessed by the final read request in the last request group,

executing said read requests in the next request group at first, and then executing other read requests in the next request group.

3. (Previously Presented) The method of claim 1 wherein the computer device comprises a memory controller that stores the plurality of read requests in a queue.

4. (Currently Amended) The method of claim 1 wherein the computer device comprises a memory controller installed in a north bridge circuit and the north bridge circuit is used for controlling transmission between a ~~display controller~~ graphics chip and the memory device.

5. (Currently Amended) The method of claim 1 wherein the computer device comprises a memory controller, and data that are read with the memory controller are transmitted to a ~~display controller~~ graphics chip.

6. (Currently Amended) The method of claim 5 wherein the ~~display controller~~ graphics chip is connected electrically to the memory controller through an accelerated graphics port bus in the computer device.

7-8. (Cancelled).

9. (Original) The method of claim 1 wherein the memory device is a system memory of the computer system.

10. (Currently Amended) The method of claim 1 wherein the computer device comprises a memory controller that stores the data in the ~~display controller~~ graphics chip according to the predetermined request sequence.

11. (Previously Presented) A method for accessing data, a plurality of read requests used for accessing data from a memory device according to a predetermined request sequence, the method comprising:

establishing at least two request groups for the plurality of read requests;

reordering said read requests according to pages in said memory device accessed by said read requests into a second request sequence, wherein within each request group, said read requests accessing the same page of said memory device are continuously arranged, and when a current request group has a read request of the same page as a last read request of a previous request group, a first read request of the current request group is ordered to correspond to the

page of the last read request of the previous request group; and

executing the read requests according to said second request sequence.

12. (Cancelled)

13. (Previously Presented) The method of claim 11 wherein a memory controller is used to store the plurality of read requests in a queue.

14. (Currently Amended) The method of claim 11 wherein a memory controller is installed in a north bridge circuit and the north bridge circuit is used for controlling the transmission between a ~~display controller~~ graphics chip and the memory device.

15. (Currently Amended) The method of claim 11 wherein data are read with a memory controller and are transmitted to a ~~display controller~~ graphics chip.

16. (Currently Amended) The method of claim 15 wherein the ~~display controller~~ graphics chip is connected electrically to the memory controller through an accelerated graphics port bus in the computer device.

17-18. (Cancelled)

19. (Original) The method of claim 11 wherein the memory device is a system memory of the computer device.

20. (Currently Amended) The method of claim 11 wherein a memory controller stores data in a ~~display controller~~ graphics chip according to the predetermined request sequence.